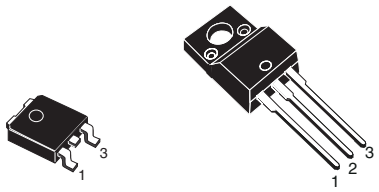
STD5N52U
STF5N52U

N-channel 525 V, 1.28 Ω, 4.4 A, DPAK, TO-220FP UltraFASTmesh™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD5N52U	525 V	< 1.5 Ω	4.4 A	70 W
STF5N52U	525 V	< 1.5 Ω	4.4 A	25 W

- 100% avalanche tested
- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}



DPAK TO-220FP

Application

- Switching applications
  - High voltage inverters specific fo LCD TV
  - Lighting full bridge topology
  - Motor control

Description

The UltraFASTmesh™ series associates all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with an extremely enhanced fast body-drain recovery diode.

Figure 1. Internal schematic diagram

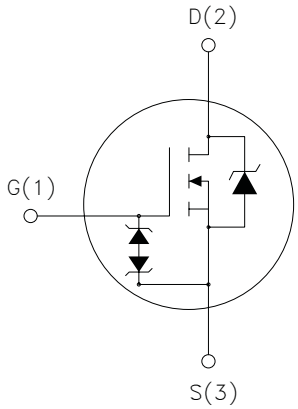


Table 1. Device summary

Order code	Marking	Package	Packaging
STD5N52U	5N52U	DPAK	Tape and reel
STF5N52U	5N52U	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	4.4		A
I_D	Drain current (continuous) at T_C = 100 °C	2.8		A
I_{DM} (1)	Drain current (pulsed)	17.6		A
P_{TOT}	Total dissipation at T_C = 25 °C	25	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.4		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170		mJ
dv/dt(2)	Peak diode recovery voltage slope	20		V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF; R=1.5 kΩ)	2800		V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500		V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 4.4 A, di/dt ≤ 400 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	5	1.78	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	100	°C/W
T_J	Maximum lead temperature for soldering purpose	300		°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.2 A		1.28	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	529 71 13.4	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 420 V, V_{GS} = 0	-	11	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	6	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 416 V, I_D = 4.4 A, V_{GS} = 10 V *(see Figure 17)*	-	16.9 4.2 8.4	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 260 V, I_D = 2.2 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 16)*	-	11.4 13.6 23.1 15	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		4.4 17.6	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.4 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 18)*	-	55 95 3.5		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 18)*	-	120 266 4.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

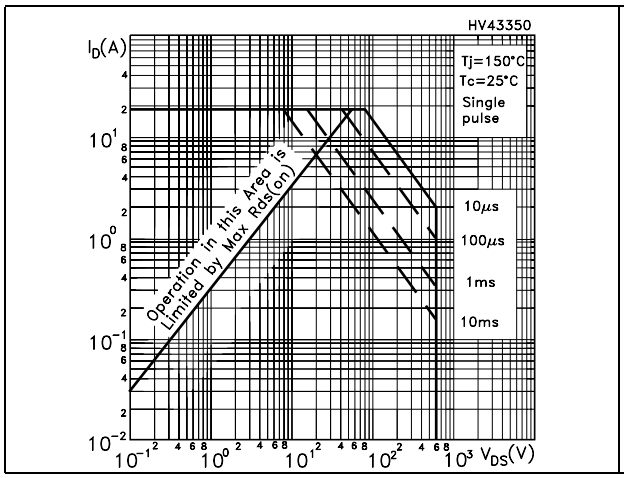


Figure 3. Thermal impedance for TO-220FP

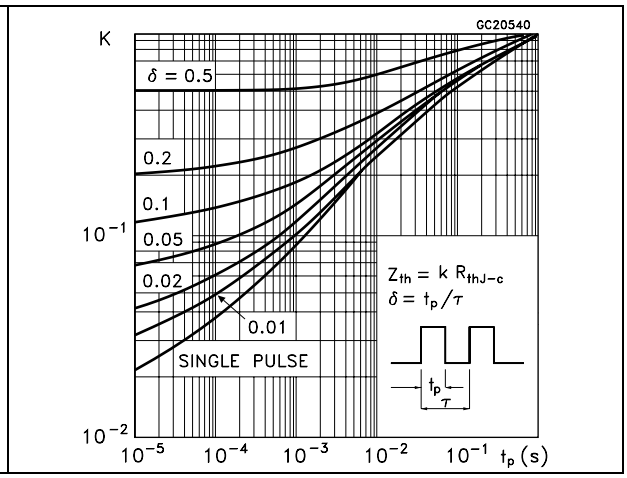


Figure 4. Safe operating area for DPAK

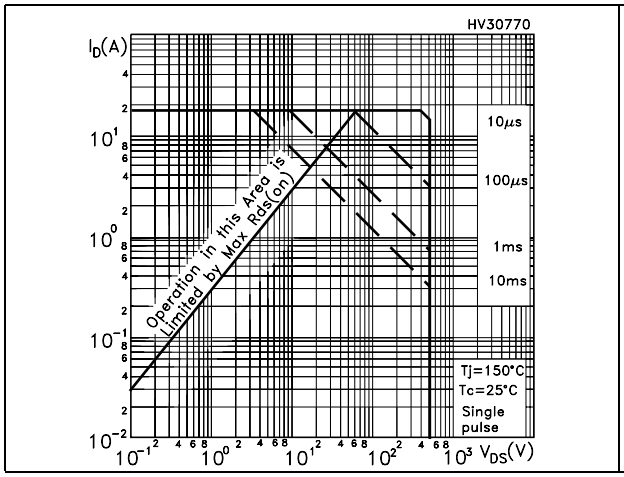


Figure 5. Thermal impedance for DPAK

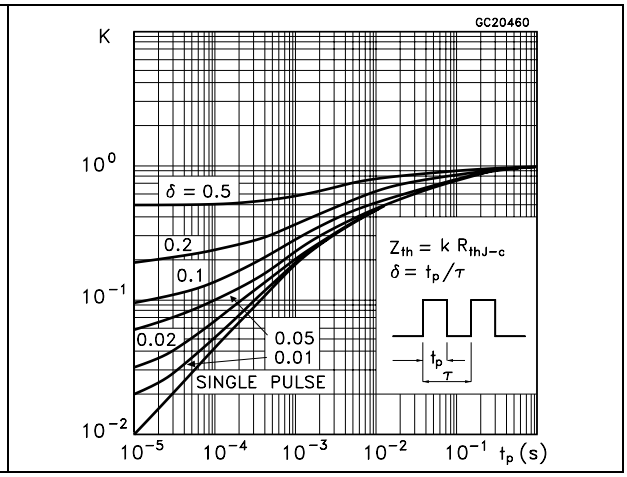


Figure 6. Output characteristics

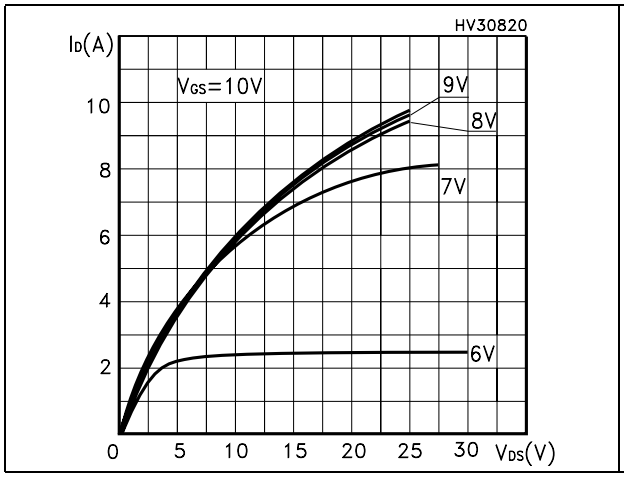


Figure 7. Transfer characteristics

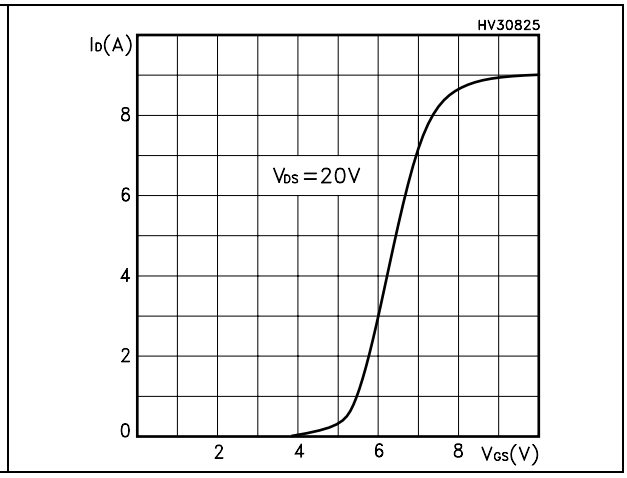


Figure 8. Normalized BV_{DSS} vs temperature

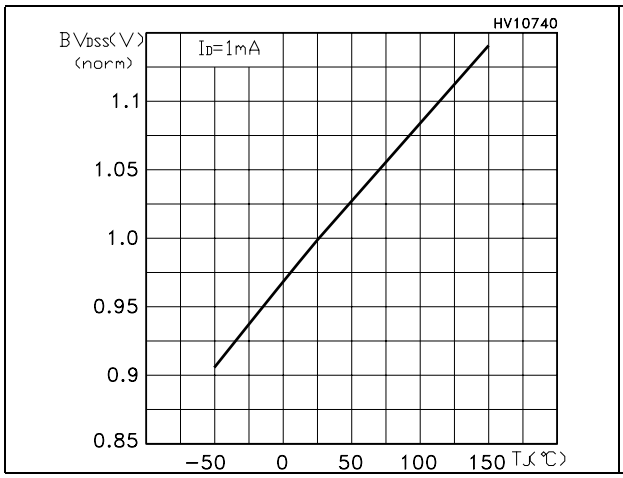


Figure 9. Static drain-source on resistance

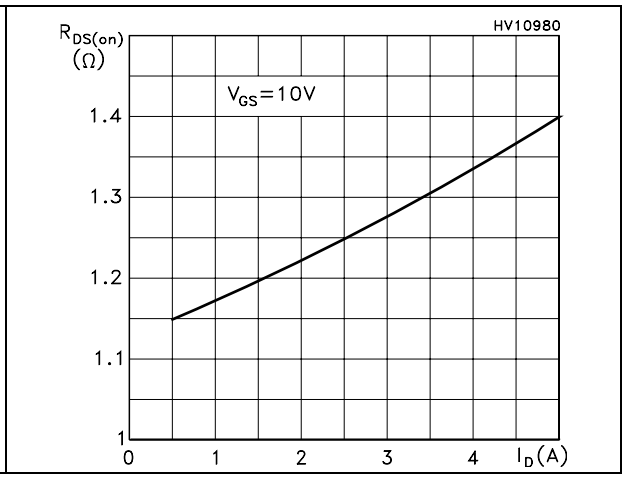


Figure 10. Gate charge vs gate-source voltage

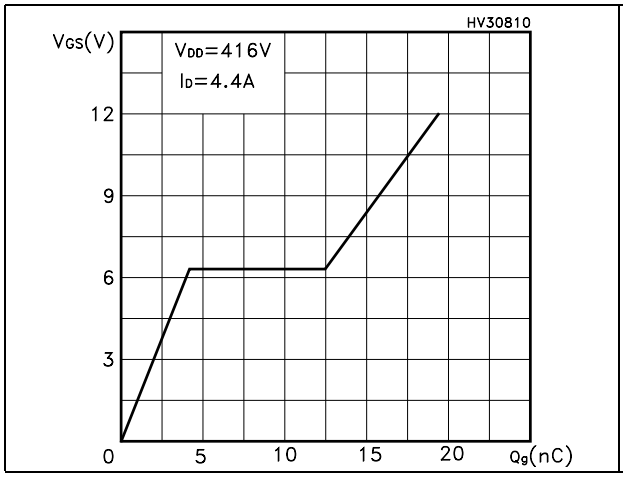


Figure 11. Capacitance variations

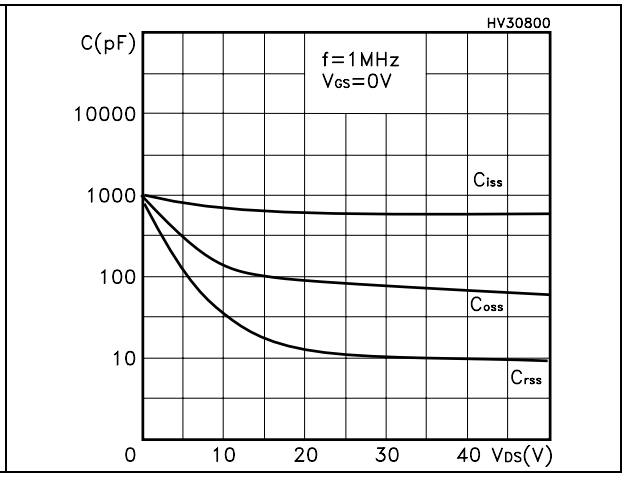


Figure 12. Normalized gate threshold voltage vs temperature

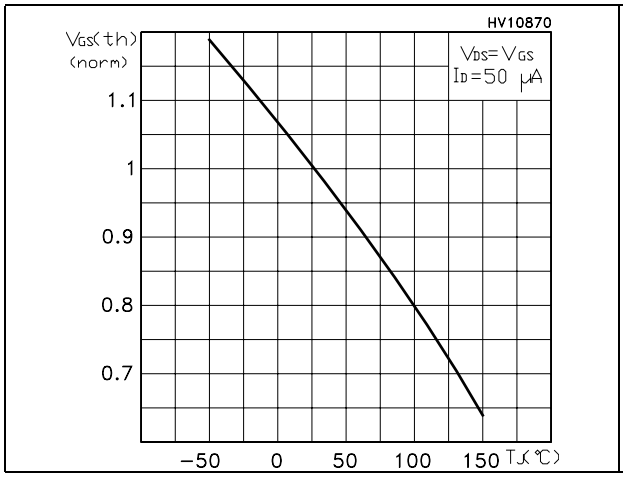


Figure 13. Normalized on resistance vs temperature

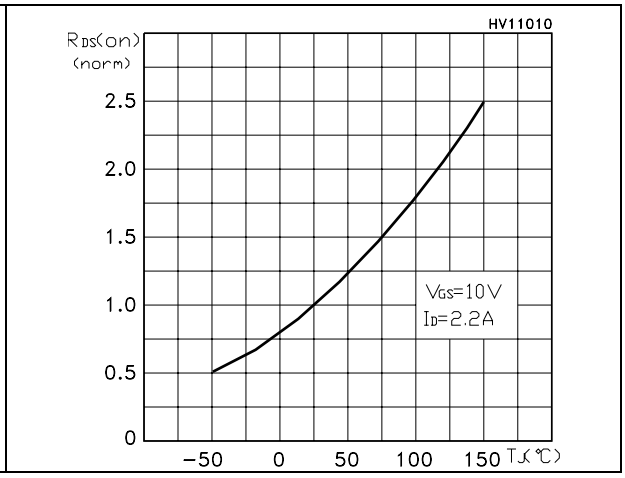


Figure 14. Source-drain diode forward characteristics

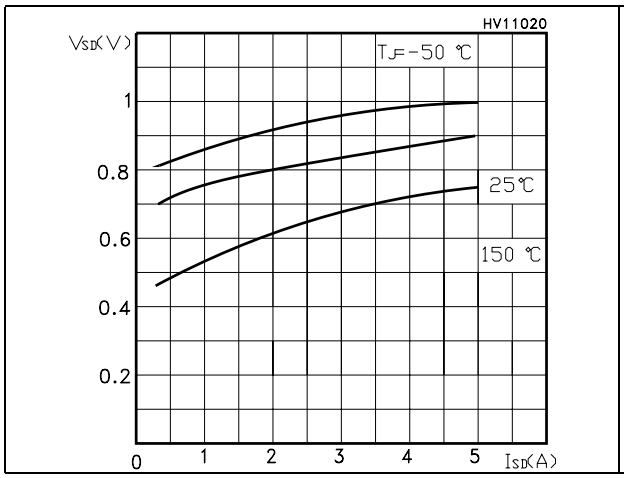
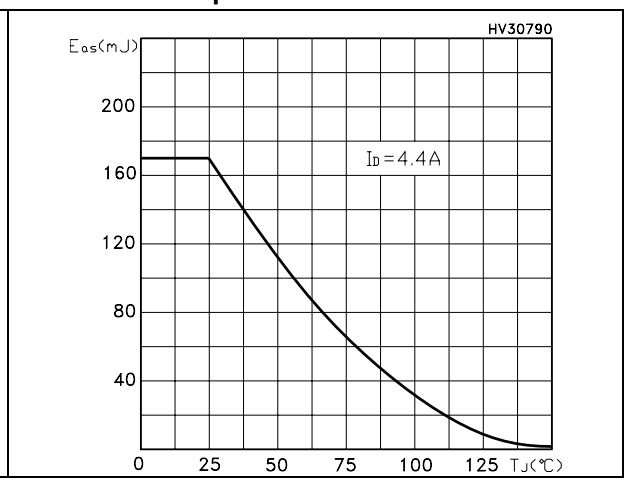


Figure 15. Maximum avalanche energy vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

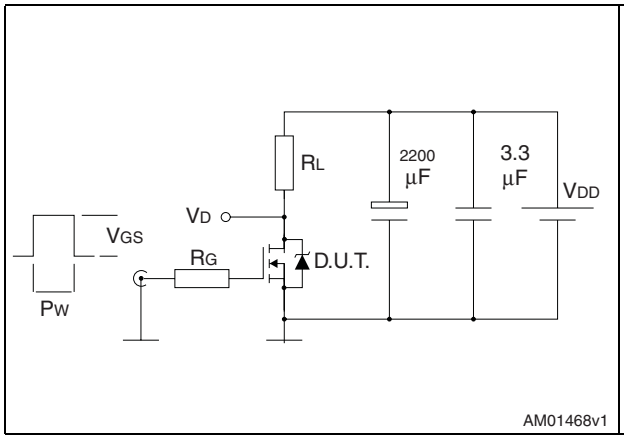


Figure 17. Gate charge test circuit

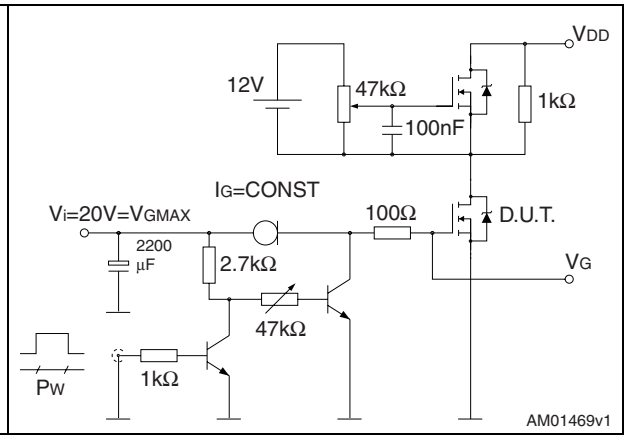


Figure 18. Test circuit for inductive load switching and diode recovery times

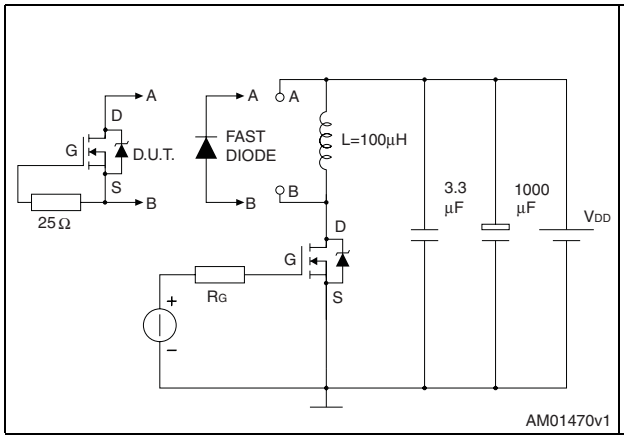


Figure 19. Unclamped inductive load test circuit

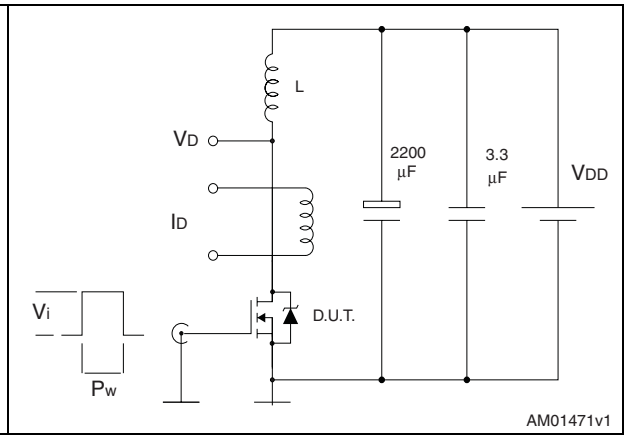


Figure 20. Unclamped inductive waveform

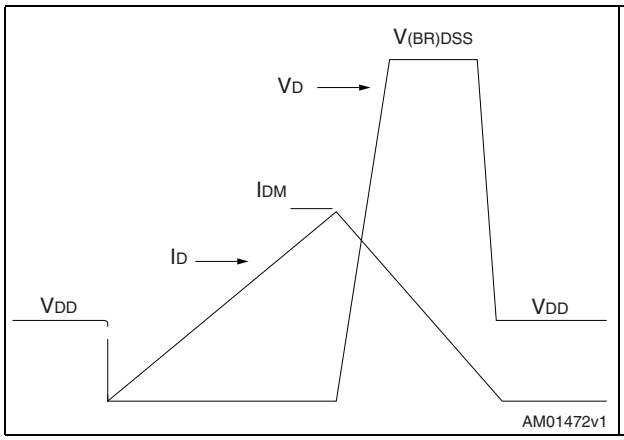
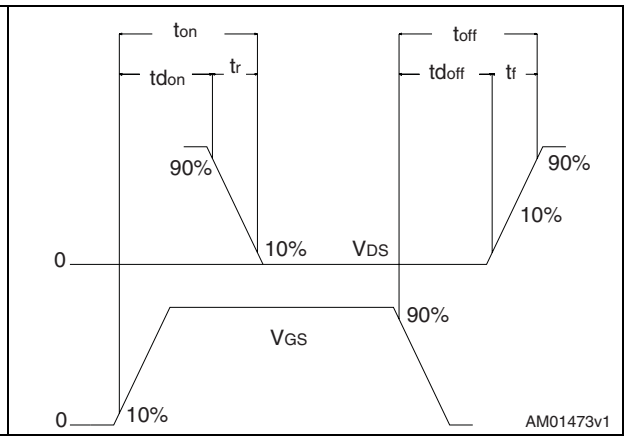


Figure 21. Switching time waveform

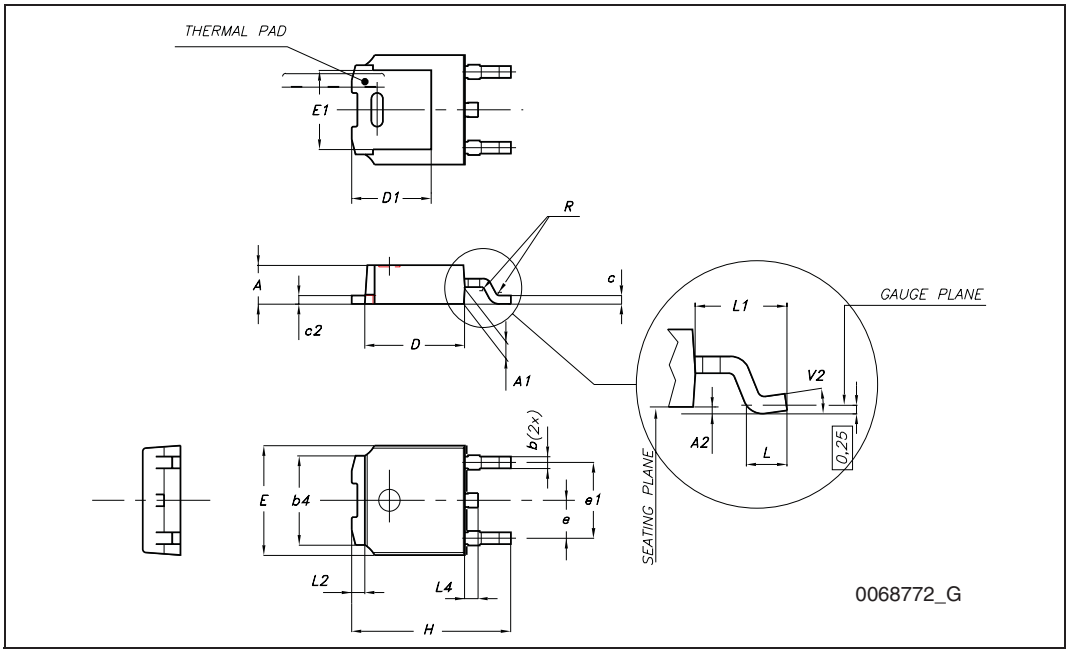


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

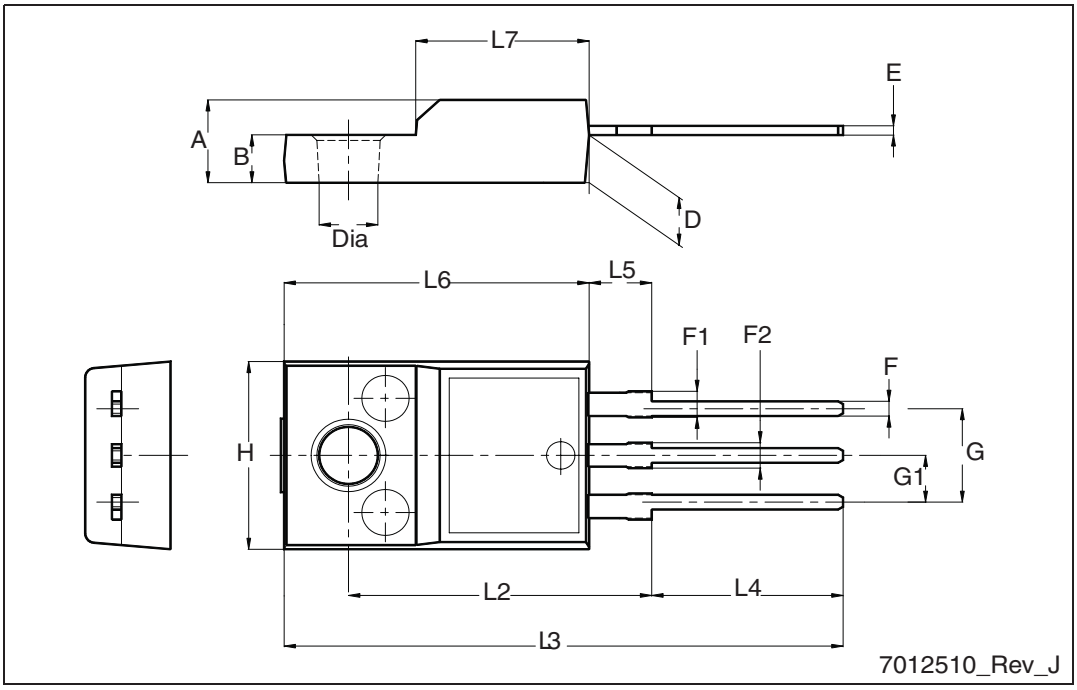
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



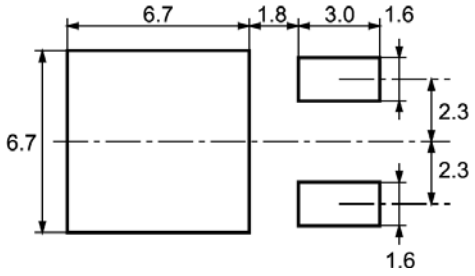
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



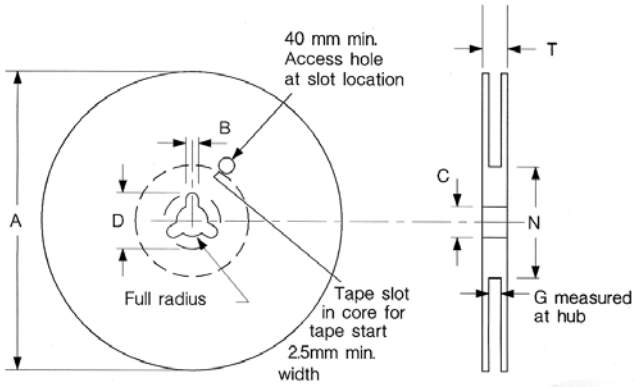
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



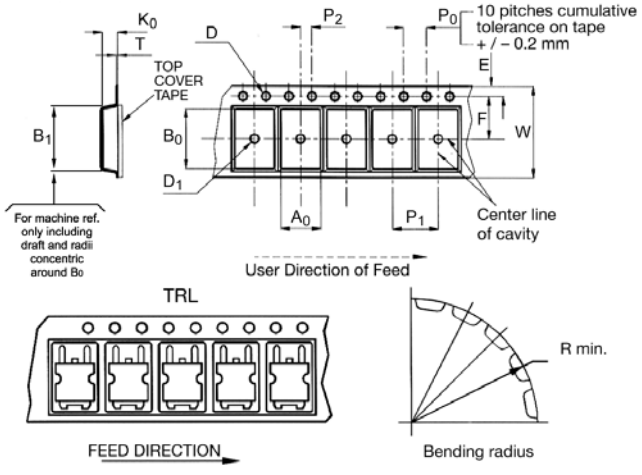
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-May-2009	1	First release

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