FAIRCHILD SEMICONDUCTOR®

June 2003

FDS6993

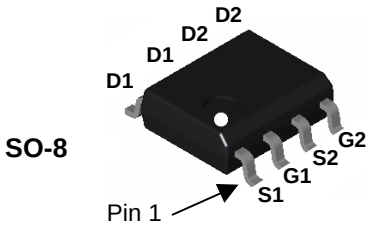
Dual P-Channel PowerTrench® MOSFET

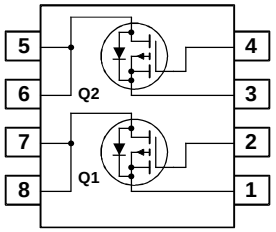
General Description

These P-Channel MOSFETs are made using FSC's **PowerTrench**® technology. They are packaged in a single SO-8 which is designed to allow two MOSFETs to operate independenly, each with it's own heat sink. The combination of silicon and package technologies results in minimum board space and cost.

Features

- **Q1**: P-Channel
  –4.3A, –30V $R_{DS(on)}$ = 55mΩ @ V_{GS} = –10V
  $R_{DS(on)}$ = 85mΩ @ V_{GS} = –4.5V
- **Q2**: P-Channel
  –6.8A, –12V $R_{DS(on)}$ = 17mΩ @ V_{GS} = –4.5V
  $R_{DS(on)}$ = 24mΩ @ V_{GS} = –2.5V
  $R_{DS(on)}$ = 30mΩ @ V_{GS} = –1.8V
- High power and handling capability in a widely used surface mount package





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		–30	–12	V
V_{GSS}	Gate-Source Voltage		±25	±8	V
I_D	Drain Current - Continuous	(Note 1a)	–4.3	–6.8	A
	- Pulsed		–20	–20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6993	FDS6993	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA V_{GS} = 0 V, I_D = –250 µA	Q1 Q2	–30 –12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		–21 –0.9		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V V_{DS} = –10 V, V_{GS} = 0 V	Q1 Q2			–1 –1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±25 V, V_{DS} = 0 V V_{GS} = ±8 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA V_{DS} = V_{GS}, I_D = –250 µA	Q1 Q2	–1 –0.4	–1.8 –0.5	–3 –1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		4 3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = –10 V, I_D = –4.3 A V_{GS} = –10 V, I_D = –4.3 A, T_J = 125°C V_{GS} = –4.5 V, I_D = –3.4 A	Q1		48 64 74	55 80 85	mΩ
		V_{GS} = –4.5 V, I_D = –6.8 A V_{GS} = –4.5 V, I_D = –6.8 A, T_J = 125°C V_{GS} = –2.5 V, I_D = –5.9 A V_{GS} = –1.8 V, I_D = –5.0	Q2		11 14 14 19	17 24 24 30	
$I_{D(on)}$	On-State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V V_{GS} = –4.5 V, V_{DS} = –5 V	Q1 Q2	–20 –20			A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –7 A V_{DS} = –5 V, I_D = –5 A	Q1 Q2		9 34		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		530 2980		pF
C_{oss}	Output Capacitance	Q2 V_{DS} = –6 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		140 1230		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		70 790		pF

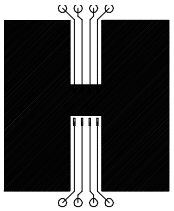
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

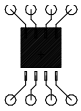
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10V, R_{GEN} = 6 Ω	Q1 Q2		10 19	19 34	ns
t_r	Turn-On Rise Time		Q1 Q2		14 20	26 35	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = –6 V, I_D = –1 A, V_{GS} = –4.5V, R_{GEN} = 6 Ω	Q1 Q2		14 134	24 215	ns
t_f	Turn-Off Fall Time		Q1 Q2		9 121	18 193	ns
Q_g	Total Gate Charge	Q1 V_{DS} = –15 V, I_D = –4.3 A, V_{GS} = –5 V Q2 V_{DS} = –6 V, I_D = –6.8 A, V_{GS} = –5 V	Q1 Q2		5.5 32	7.7 45	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		1.8 4.0		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		2.2 8.0		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			–1.3 –1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.3 A (Note 2) V_{GS} = 0 V, I_S = –1.3 A (Note 2)	Q1 Q2		–0.8 –0.6	–1.2 –1.2	V

Notes:

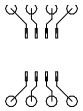
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°/W when mounted on a .02 in^2 pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics: Q1

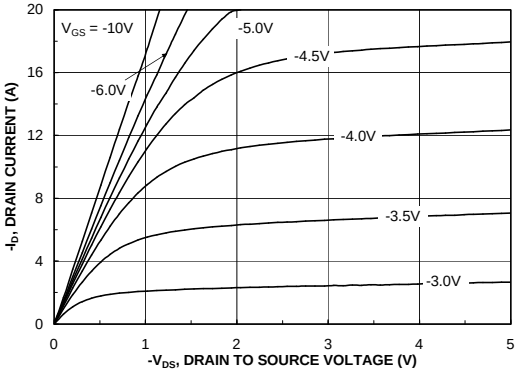


Figure 1. On-Region Characteristics.

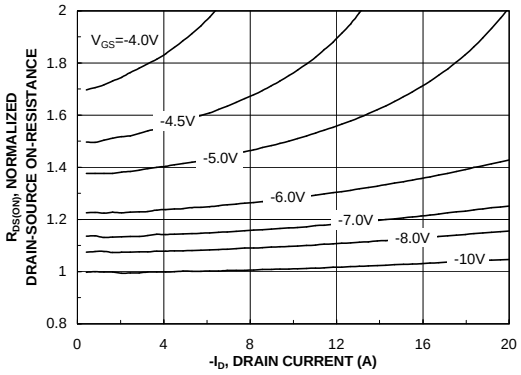


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

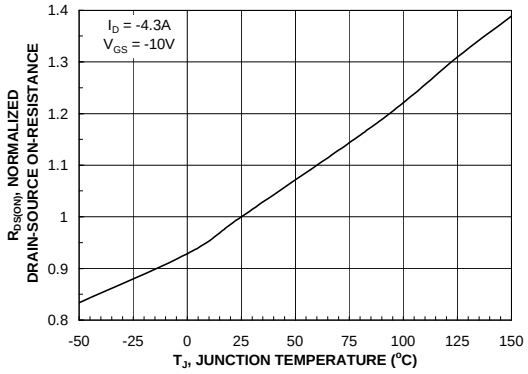


Figure 3. On-Resistance Variation with Temperature.

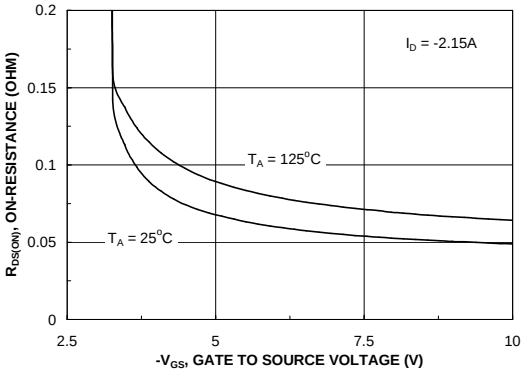


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

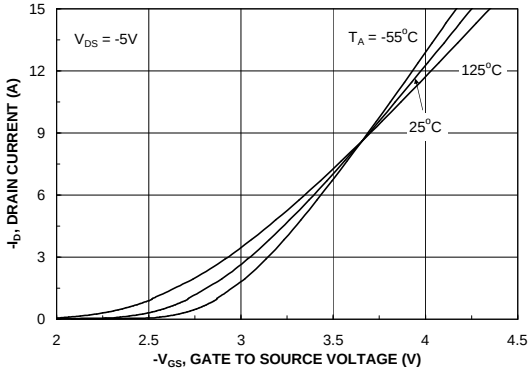


Figure 5. Transfer Characteristics.

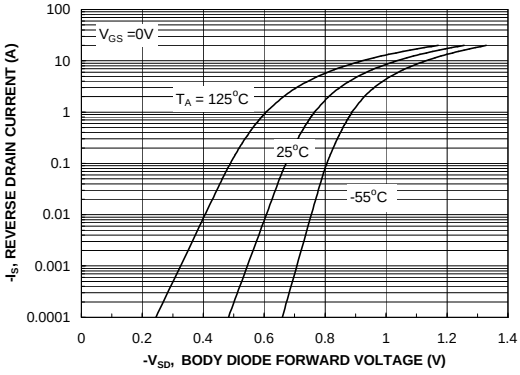


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

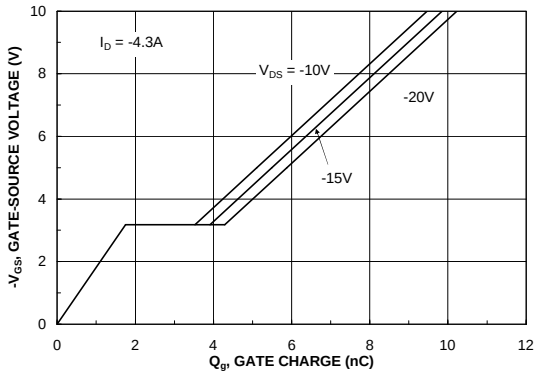


Figure 7. Gate Charge Characteristics.

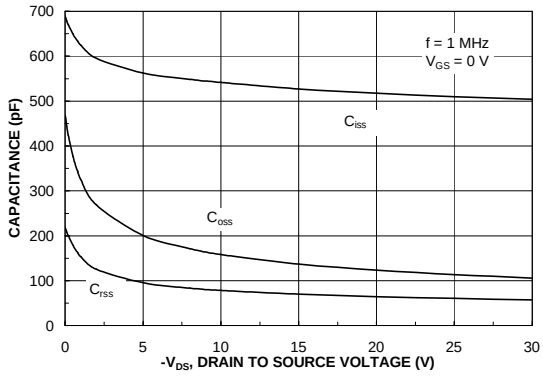


Figure 8. Capacitance Characteristics.

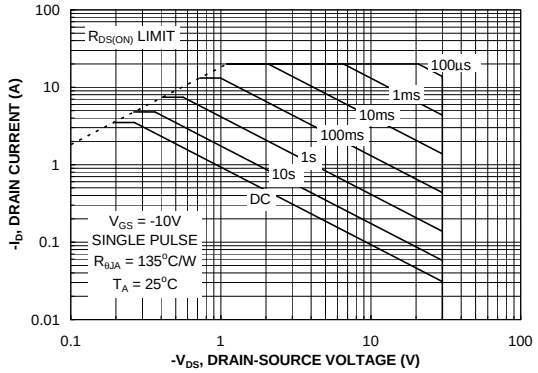


Figure 9. Maximum Safe Operating Area.

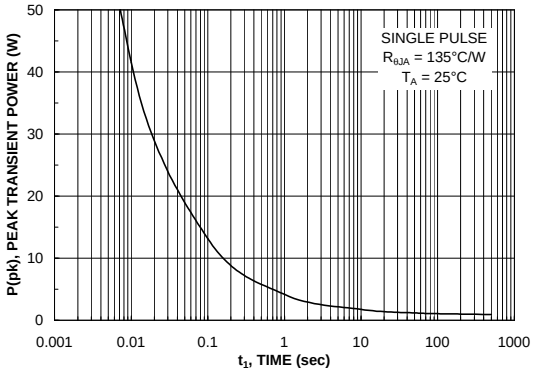


Figure 10. Single Pulse Maximum Power Dissipation.

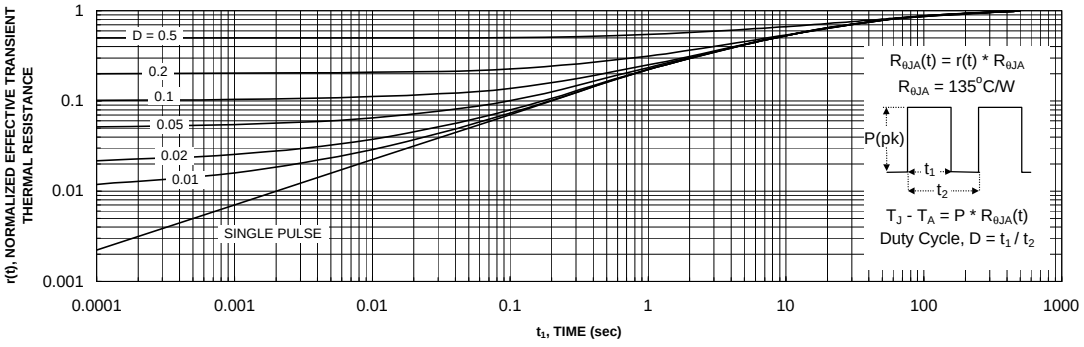


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics: Q2

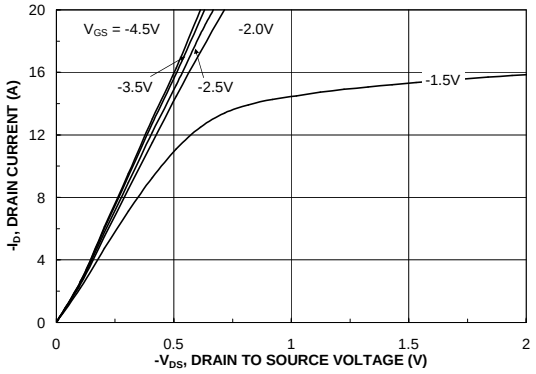


Figure 12. On-Region Characteristics.

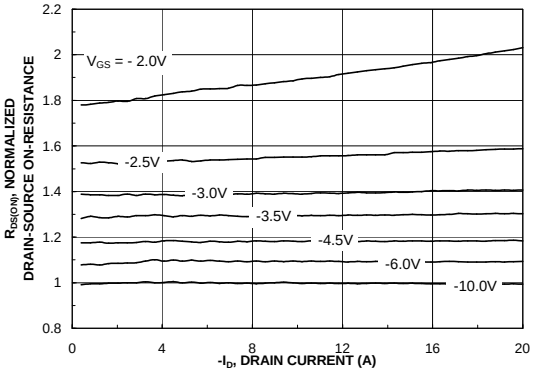


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

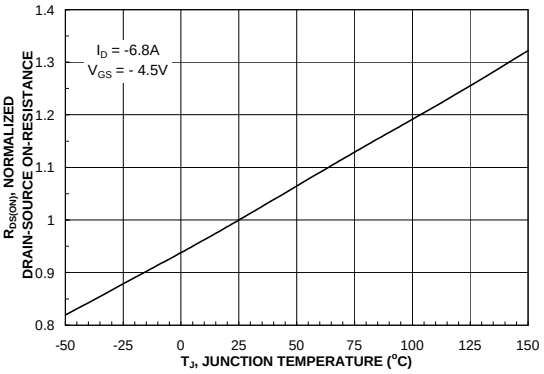


Figure 14. On-Resistance Variation with Temperature.

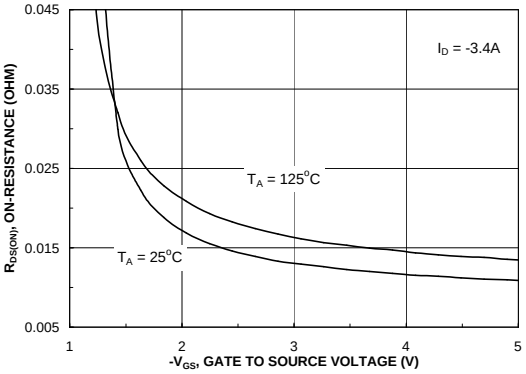


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

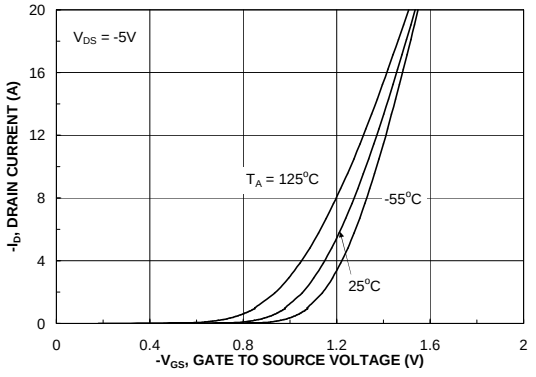


Figure 16. Transfer Characteristics.

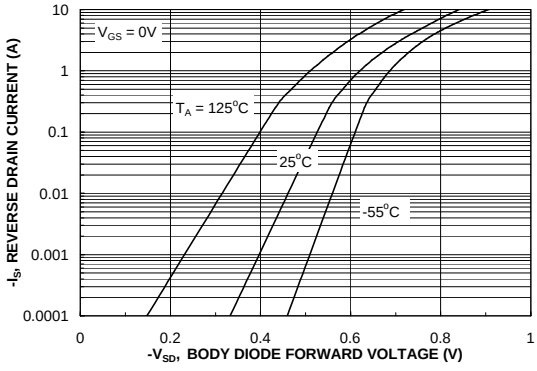


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

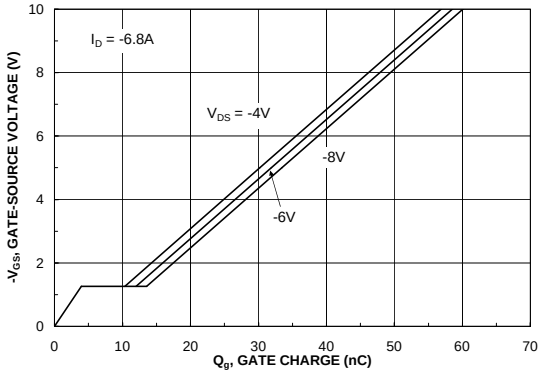


Figure 18. Gate Charge Characteristics.

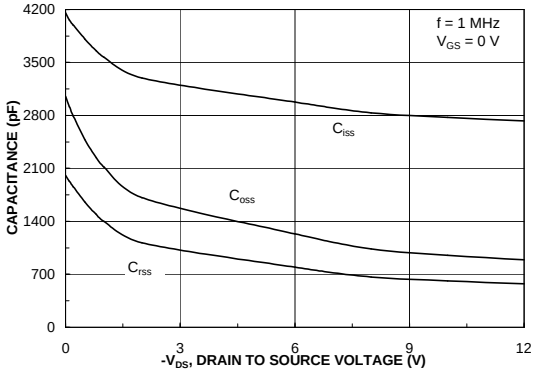


Figure 19. Capacitance Characteristics.

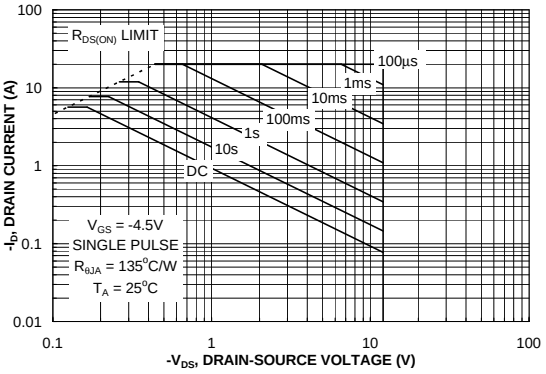


Figure 20. Maximum Safe Operating Area.

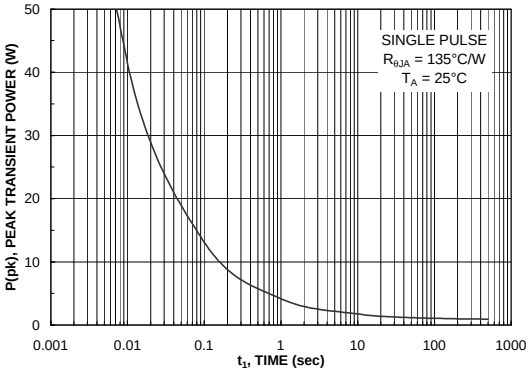


Figure 21. Single Pulse Maximum Power Dissipation.

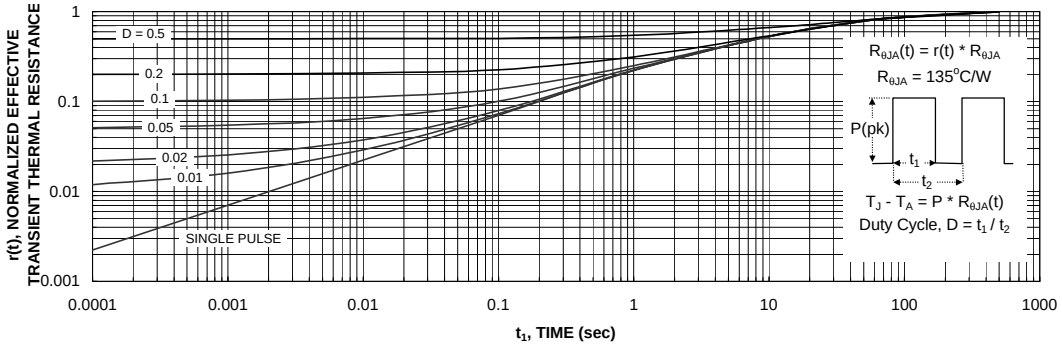


Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.