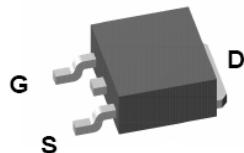


P4404EDG

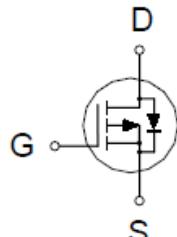
P-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	44mΩ @ $V_{GS} = -10V$	-20A



TO-252



100% UIS tested
100% Rg tested

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	-20	A
		-16	
Pulsed Drain Current ¹	I_{DM}	-50	
Avalanche Current	I_{AS}	-18	
Avalanche Energy ²	E_{AS}	48	mJ
Power Dissipation	P_D	30	W
		19	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		4.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$		80	

¹Pulse width limited by maximum junction temperature.

² $V_{DD} = -20V$, Starting $T_J = 25^\circ C$.

P4404EDG

P-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.7	-1.9	-2.5	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -32\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = -30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{\text{D}(\text{ON})}$	$V_{\text{DS}} = -5\text{V}, V_{\text{GS}} = -10\text{V}$	-50			A
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = -4.5\text{V}, I_D = -8\text{A}$		57	68	$\text{m}\Omega$
		$V_{\text{GS}} = -10\text{V}, I_D = -10\text{A}$		38	44	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = -10\text{V}, I_D = -10\text{A}$		11		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -20\text{V}, f = 1\text{MHz}$		850		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge ²	Q_g	$V_{\text{DS}} = 0.5V_{(\text{BR})\text{DSS}}, V_{\text{GS}} = -10\text{V}, I_D = -10\text{A}$		14		nC
Gate-Source Charge ²	Q_{gs}			2.2		
Gate-Drain Charge ²	Q_{gd}			1.9		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		3.5	5	Ω
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = -20\text{V}, R_L = 1\Omega$ $I_D \approx -1\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GS}} = 6\Omega$		6.0	12.8	nS
Rise Time ²	t_r			9.2	18.6	
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			19.2	34.8	
Fall Time ²	t_f			11.8	21.6	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				-20	A
Forward Voltage ¹	V_{SD}	$I_F = -10\text{A}, V_{\text{GS}} = 0\text{V}$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		15.5		nS
Reverse Recovery Charge	Q_{rr}			7.9		nC

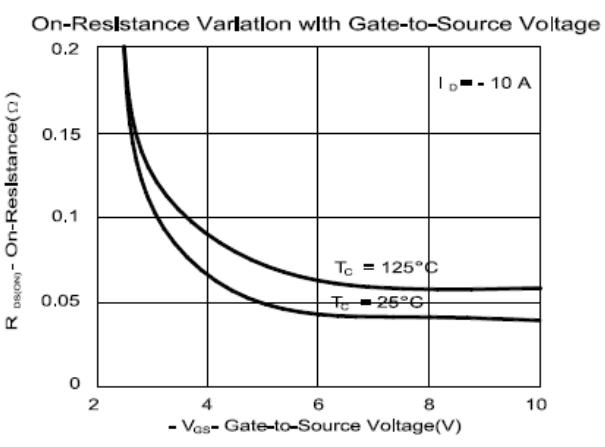
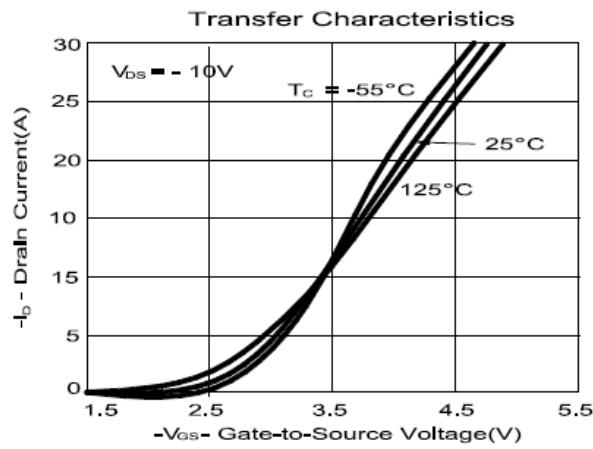
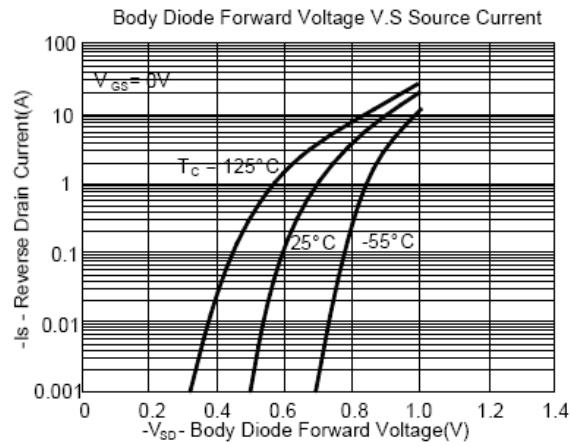
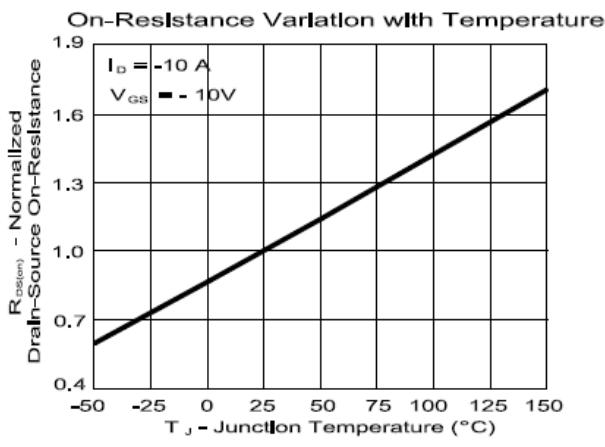
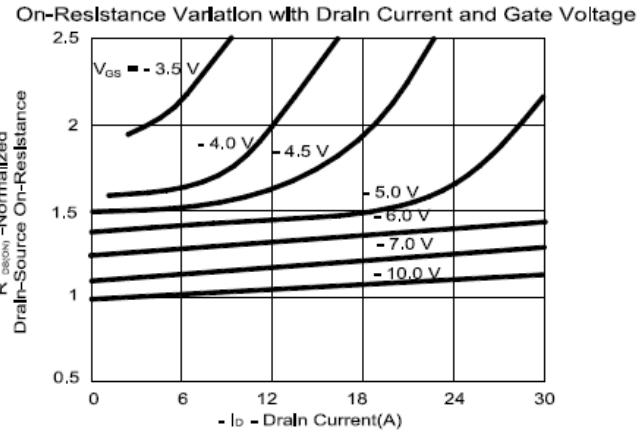
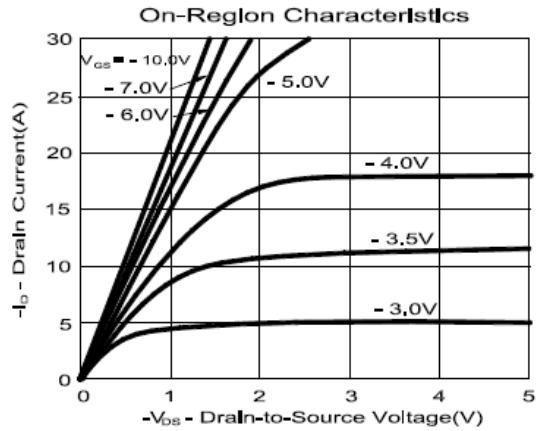
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

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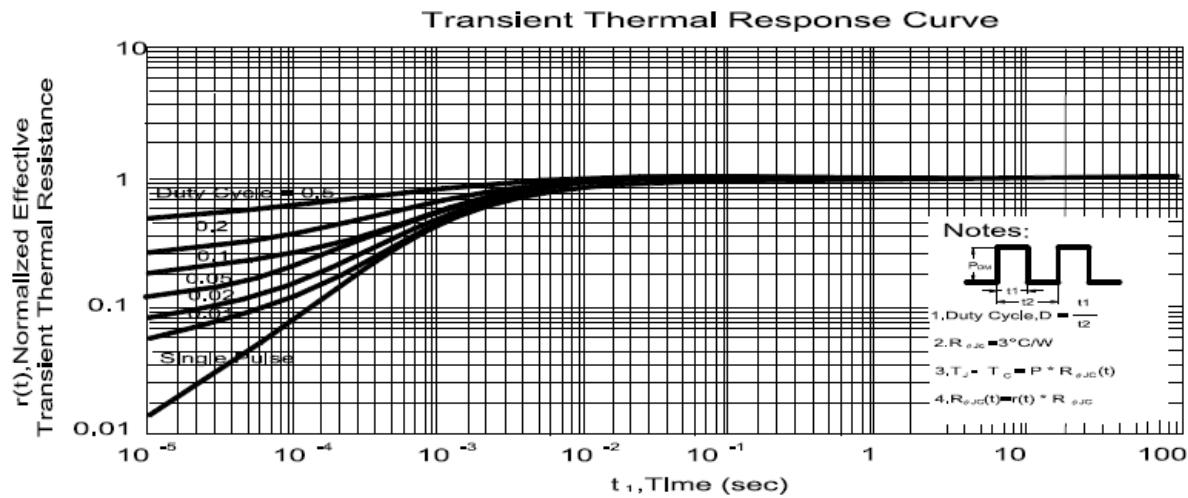
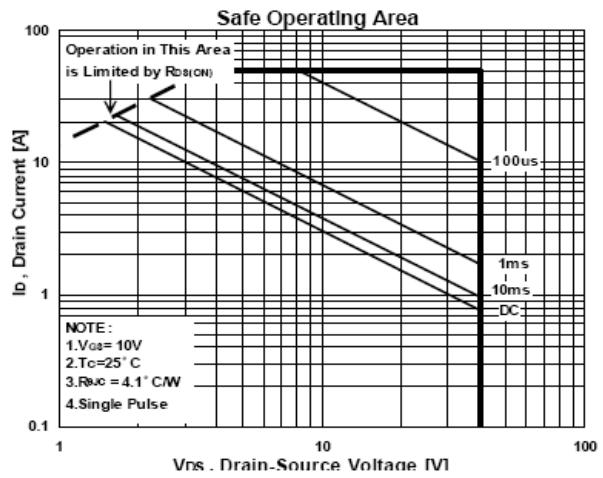
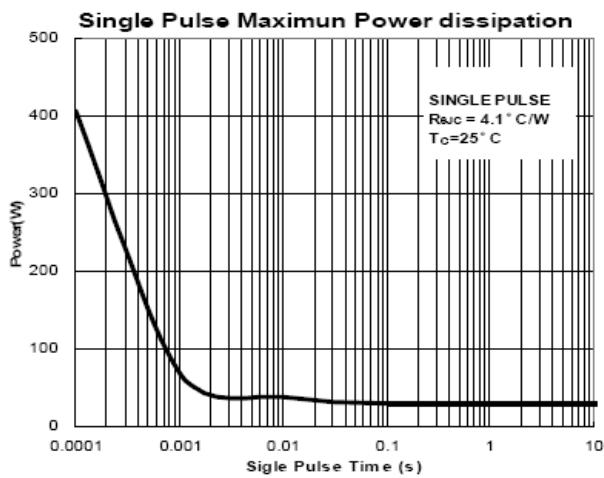
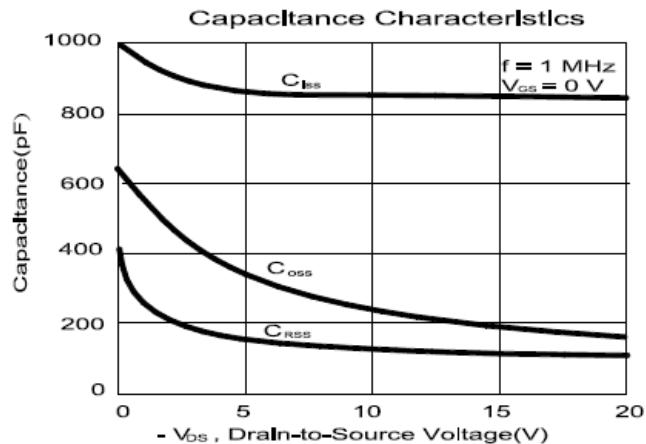
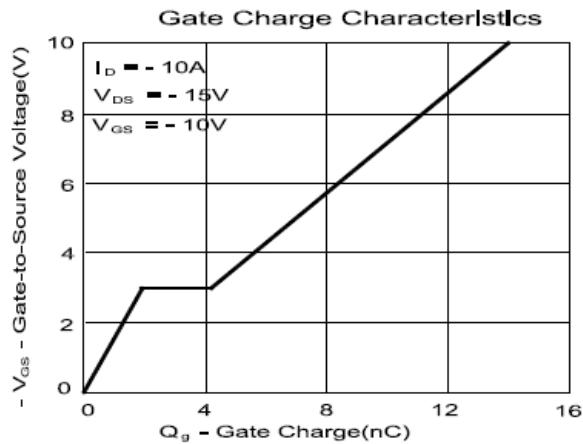
P-Channel Enhancement Mode MOSFET

TYPICAL PERFORMANCE CHARACTERISTICS



P4404EDG

P-Channel Enhancement Mode MOSFET



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P-Channel Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.5	K	0.15		1.49
C	0.4	0.5	0.61	L	0.4	0.76	0.91
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.35	0.5	0.65	S	4.57	5.1	5.52
F	0		0.2	T	3.81	4.75	5.24
G	5.3	6.1	6.3	U	1.4		1.78
H	0.5		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				

